Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MILTON LIE

Appeal No. 1999-0014
Application No. 08/748,123

ON BRIEF

Before KRASS, GROSS, and BARRY, Administrative Patent Judges.
GROSS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 1 through 3, 5 through 10, 12 through 16, and 18 through 21, which are all of the claims pending in this application. Claims 4, 11, and 17 have been canceled.

Appellant's invention relates to a processor with hardware for expediting bit scan instructions. In particular the output bits of the output destination index are simultaneously calculated and presented in parallel without requiring resolution of any bits before resolving any other

bits. Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. A computer processor comprising:

a register file including a plurality of physical registers; and,

an execution unit that executes bit scan instructions, coupled to the register file and having a leading/trailing zero detector circuit for receiving a source operand from the register file and detecting in parallel, which bit positions in the source operand are non-zero, and providing an output destination index having a plurality of bits, to indicate a first non-zero bit position in the source operand wherein the plurality of bits of the output destination index are simultaneously calculated and presented in parallel without requiring resolution of any of the plurality of bits before resolving any other of the plurality of bits.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Hannai	4,833,348	May 23, 1989
Watanabe et al. (Watanabe)	5,091,874	Feb. 25, 1992

Claims 1 through 3, 5, 7 through 10, 12 through 16, and 18 through 21 stand rejected under 35 U.S.C. § 103 as being unpatentable over Watanabe.

Claim 6 stands rejected under 35 U.S.C. § 103 as being unpatentable over Watanabe in view of Hannai.

Reference is made to the Examiner's Answer (Paper No. 16, mailed February 6, 1998) for the examiner's complete reasoning in support of the rejections, and to appellant's Brief (Paper No. 15, filed December 17, 1997) for appellant's arguments thereagainst.

OPINION

We have carefully considered the claims, the applied prior art references, and the respective positions articulated by appellant and the examiner. As a consequence of our review, we will reverse the obviousness rejections of claims 1 through 3, 5 through 10, 12 through 16, and 18 through 21.

Appellant argues (Brief, pages 5-6) that Watanabe's zero detector output is not simultaneously calculated as recited in each of independent claims 1, 8, 14, 20, and 21. The examiner responds (Answer, pages 4-5) that

> the degree of "simultaneously calculated" is the same in Watanabe's zero detector as it is in appellant's zero detector. Appellant's Fig. 6 clearly shows that the zero detector output bits <2:0> are generated before the zero detector output bits <5:3> because the signals that select the <2:0>

> bits are generated before the <5:3> bits, note selection unit 212.

In other words, the examiner admits that Watanabe's zero detector output is not simultaneously calculated and, therefore, fails to meet the claim limitation. We also note that contrary to the examiner's assertion, output bits <2:0> and output bits <5:3> in appellant's Figure 6 do appear to be calculated simultaneously, as they are output to a common node, and bits <5:0> are output from the common node. Accordingly, the examiner has failed to establish a *prima facie* case of obviousness, and we cannot sustain the rejection of claims 1 through 3, 5, 7 through 10, 12 through 16, and 18 through 21.

As to claim 6, the examiner combines Hannai with Watanabe. However, claim 6 depends from claim 1, and, therefore, includes the limitation above found lacking from Watanabe that the zero detector output must be simultaneously calculated. Hannai fails to cure this deficiency. Consequently, we cannot sustain the obviousness rejection of claim 6.

CONCLUSION

The decision of the examiner rejecting claims 1 through 3, 5 through 10, 12 through 16, and 18 through 21 under 35 U.S.C. § 103 is reversed.

REVERSED

ERROL A. KRASS Administrative Patent Judge	)	
ANITA PELLMAN GROSS Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
LANCE LEONARD BARRY Administrative Patent Judge	)	

apg/vsh

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